

Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	09/724,585
				Filing Date	11/28/2000
				First Named Inventor:	John M. Beardslee
				Art Unit	2123
				Examiner Name	Thangavelu, K.
Sheet	1	of	7	Attorney Docket No.	02986.P035

U.S. PATENT DOCUMENTS						
Exmnr Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
A		US- 6,587,995	B1	07/01/2003	Duboc et al.	
		US- 6,779,145	B1	08/17/2004	Edwards et al.	
I		US- 6,785,854	B1	08/31/2004	Jaramillo et al.	
		US- 6,789,217	B2	09/07/2004	Slaugh et al.	
K/M/N		US- 6,791,352	B2	09/14/2004	Verdoorn et al.	
		US- 6,795,963	B1	09/21/2004	Andersen et al.	
		US- 6,799,128	B2	09/28/2004	Duff et al.	
		US- 6,822,474	B2	11/23/2004	Chaudhari	
		US- 6,823,224	B2	11/23/2004	Wood et al.	
		US- 6,826,717	B1	11/30/2004	Draper et al.	
		US- 6,839,654	B2	01/04/2005	Röllig et al.	
		US- 6,839,874	B1	01/04/2005	Fang	
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		US- 6,868,376	B2	03/15/2005	Swoboda	
✓		US- 6,894,530	B1	05/17/2005	Davidson et al.	

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		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
↑ KRM ↓		WIPO	00/043884	A1	07/27/2000	Wenzel et al.		
		WIPO	01/063434	A1	08/30/2001	Barry		
		WIPO	01/071876	A1	09/27/2001	Ricchetti et al.		

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collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the PTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including nering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

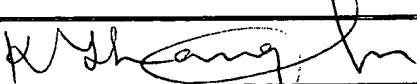
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↑		US- 6,895,365	B2	05/17/2005	Voorhees et al.	
KCM		US- 6,895,372	B1	05/17/2005	Knebel et al.	
		US- 6,904,577	B2	06/07/2005	Schubert et al.	
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↓		US- 2004/0181385	A1	09/16/2004	Milne et al.	
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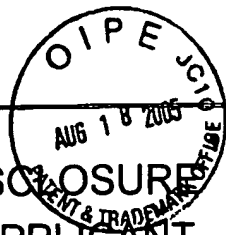
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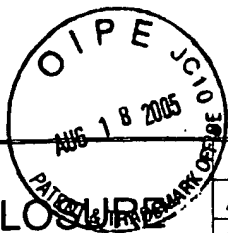


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↑		Ableidinger et al., "Multi-Core Embedded Debug for Structured ASIC Systems", DesignCon 2004, February 2004, 23 pgs.			
		"Actel Corporation, "Actel Silicon Explorer II - User's Guide", March 2004; cover page, page ii and pp.3-43.			
KM		Altera Corporation, "Quartus II Handbook, Volume 3", Section IV-1, May 2005; pp. 9/1-9/14; pp. 10/1-10/46; pp. 11/1-11/46; pp. 12/1-12/10.			
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		Bennetts, R.G., "Boundary Scan Tutorial", ASSET Intertech Inc., September 2002, pp. 1-58.			
		First Silicon Solutions, Technical Data for CLAM System for Actel FPGA Devices", http://www.fs2.com , June 2005, 2 pgs.			
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		First Silicon Solutions, Inc., "Getting Started - FS2 System Analyzer for QuickLogic Eclipse Devices", http://www.fs2.com , January 2004, pp. 1-29.			
		First Silicon Solutions, Inc., "Getting Started - System Analyzer for AMD Geode GX and Geode LX Processors", http://www.fs2.com , May 2005, pp. 1-45.			
	First Silicon Solutions, Inc., "Technical Data for ISA-ACTEL51 In-Target System Analyzer for Actel Core8051 Microcontroller Cores", http://www.fs2.com , June 2005, 2 pgs.				

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NON PATENT LITERATURE DOCUMENTS

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↑		First Silicon Solutions, Inc., "Technical Data for ISA-ARM System Analyzer for ARM Processors and Cores", http://www.fs2.com , June 2005, 2 pgs.	
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KMY		First Silicon Solutions, Inc., "Technical Data for System Navigator OE for AMD Geode GX Processors", http://www.fs2.com , June 2005, 2 pgs.	
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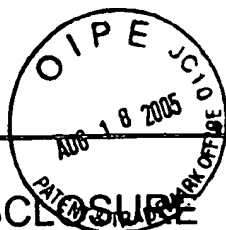
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↑		First Silicon Solutions, Inc., "NIOS II Software User Guide - System Analyzer for the Nios II Processor Core", http://www.fs2.com , November 2004, pp. 1-34.	
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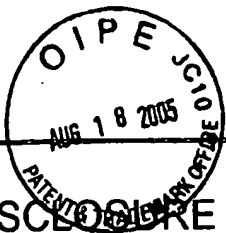
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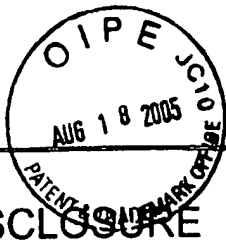
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KMN		Yang et al., "Extraction Error Modeling and Automated Model Debugging in High-Performance Low Power Custom Designs", Date Conference 2005, March 2005, 6 pgs.			

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